

Appl. No. 10/678,028
Amdt. dated Jan. 25, 2006
Reply to Office action of Nov. 3, 2005

Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig. 5. This sheet, which includes Figs. 4-6, replaces the original sheet including Fig. 4-6. In Figure 5, previously omitted reference "d" has been added.

Attachment: Replacement Sheet

Annotated Sheet Showing Changes.

Remarks

Applicants thank Examiner Doan for her careful examination of this application, the clear explanation of the claim rejections, the objection to the drawings, to the title, and to claims 2 and 13; and for conditionally allowing claims 13-15. In response, applicants amend the title, the objected drawing and the specification in this application to eliminate the informalities; and amends claims to overcome the claim rejections:

1. The title is changed application from "A LOW NOISE VERTICAL VARIABLE GATE CONTROL VOLTAGE JFET DEVCIE IN A BICMOS PROCESS AND METHODS TO BUILD THIS DEVICE" to "AN INTEGRATED CIRCUIT DEVICE WITH A VERTICAL JFET." This title is descriptive and is clearly indicative of the invention to which the claims are directed.
2. The drawing Fig. 5 is amended to incorporate the reference sign "d". Replacement sheet and an annotated sheet showing the change are attached with this paper.
3. Claims 2 is amended to add ":" after the word "comprising" and claim 13 is amended to replace "the drain plug" with "a drain plug."
4. Claim 2 is amended to add the following elements of limitations:
 - a. a vertical JFET;
 - b. the gate terminal, the source terminal, and the drain terminal all being near the top surface of the substrate; and
 - c. the JFET operable to pass an electric current between the source terminal and the drain terminal, the electric current flowing in the channel region in a direction vertical to the top and bottom surfaces of the channel region.

The added elements of limitation clearly distinguishes claim 2 over the cited references:

The Nishizawa (U.S. Pat. 4,404,575) – the '575 patent.

The '575 patent discloses a semiconductor device that has a particular current versus voltage characteristics and a small output resistance. Among the 16 embodiments in the '575 patent, not one has all the elements of limitation in claim 2 of the distant application.

Embodiments depicted in Figs. 1, 3, 6, 7, 8, 9, 10, 11, 12, 16, 20, 21, 22, and 24C do not have both the source and drain terminals near the top surface of the substrate; and embodiments depicted in Figs. 24A, 24B, and 24C are not JFETs but MOSFETs with the current paths parallel the substrate surface in Figs. 24A and 24B. Therefore the amended claim 2 overcomes the 102 rejection over the '575 patent.

The Nishizawa (U.S. Pat. 4,338,618) – the '618 patent.

As noted in the Office Action, Nishizawa '618 does not disclose that the drain region 115 can serve as a source region, and the source region 113 can serve as a drain region, and the '575 patent teaches an inverse operation. However, both patents do not disclose a JFET with a vertical channel current and having both the source and drain terminals near the top of the substrate. Therefore the amended claim 2 overcomes the 103 rejection over the '618 patent in view of the '575 patent.

5. Claim 3 is amended to delete the elements of limitation that are incorporated in the base claim 2.
6. Claim 6 limits the dopant of the NBL to antimony. The antimony doped NBL has a distinct structure that is different from other doped NBL. In the art of semiconductor device, it is well known that semiconductor doped with antimony is structurally and functionally differently from semiconductor doped with other elements. Therefore, because both '618 and '575 patents do not disclose this element, the rejection against claim 6 is improper.

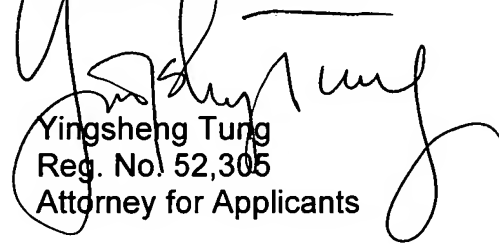
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7. Claims 3-5, 7-12 properly depend from patentable claim 2 and they stand patentable by virtue of their dependence.

Applicants respectfully submit that this application is now in allowable form and respectfully request timely allowance of all pending claims.

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Respectfully submitted,



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(ST) Repl. Sheet

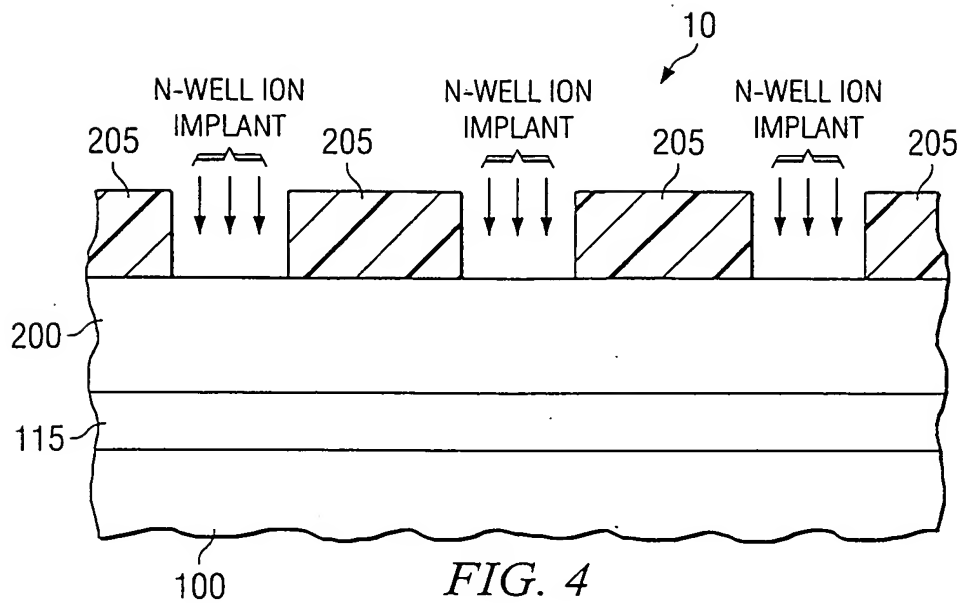


FIG. 4

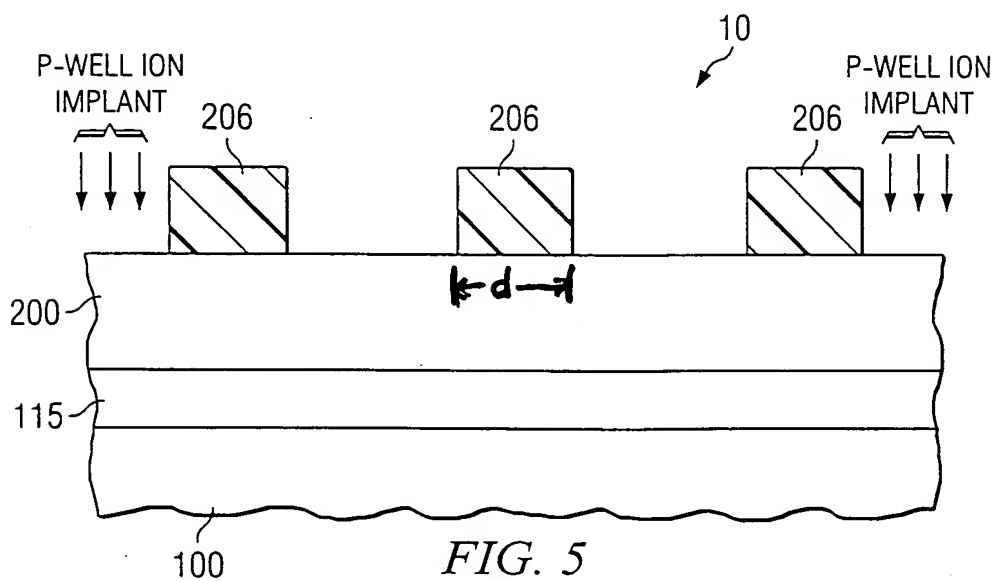


FIG. 5

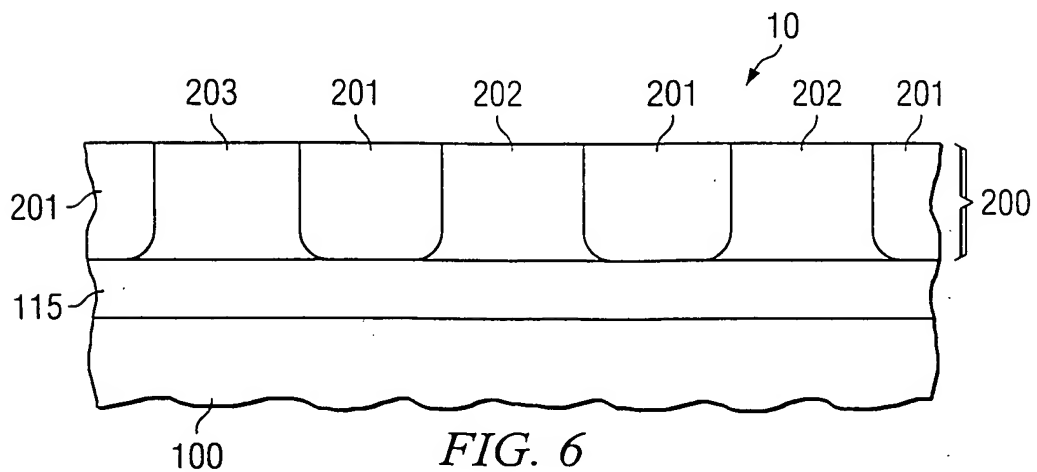


FIG. 6